AMMC-5618

6-20 GHz Amplifier

Description

AMMC-5618 is an efficient two stage amplifier designed to be use as a cascadable intermediate gain block for EW application. In communication systems, it can be use as a LO buffer or as a transmit driver amplifier.

The MMIC is a cost effective alternative to hybrid (discrete FET) amplifiers that require complex tuning and assembly processes.

Lead (PB) Free RoHS 6 fully compliant

Lifecycle status: **Active**

Features

- High Gain: 14.5 dB typical
- Output Power: 19.5 dBm typical
- Input and Output Return Loss: < -12 dB
- Flat Gain Response: /- 0.3 dB typical
- Single Supply Bias: 5 V @ 107 mA

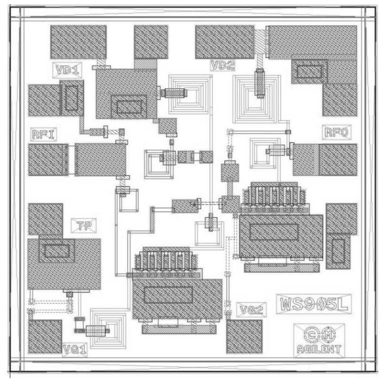
Applications

- Driver/Buffer in microwave communication systems
- Cascadable gain stage for EW systems
- Phased array radar and transmit amplifiers

AMMC - 5618

6 - 20 GHz Amplifier

Data Sheet



Chip Size: 920 x 920 µm (36.2 x 36.2 mils)
Chip Size Tolerance: ± 10µm (±0.4 mils)
Chip Thickness: 100 ± 10µm (4 ± 0.4 mils)
Pad Dimensions: 80 x 80 µm (3.1 x 3.1 mils or larger)

Description

Avago Technologies' AMMC-5618 6-20 GHz MMIC is an efficient two-stage amplifier designed to be used as a cascadable intermediate gain block for EW applications. In communication systems, it can be used as a LO buffer, or as a transmit driver amplifier. It is fabricated using a PHEMT integrated circuit structure that provides exceptional efficiency and flat gain performance. During typical operation with a single 5-V supply, each gain stage is biased for Class-A operation for optimal power output with minimal distortion. The RF input and output have matching circuitry for use in 50-W environments. The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. For improved reliability and moisture protection, the die is passivated at the active areas. The MMIC is a cost effective alternative to hybrid (discrete FET) amplifiers that require complex tuning and assembly processes.

Applications

- Driver/Buffer in microwave communication systems
- Cascadable gain stage for EW systems
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Features

- Frequency Range: 6 - 20 GHz
- High Gain: 14.5 dB Typical
- Output Power: 19.5 dBm Typical
- Input and Output Return Loss: < -12 dB
- Flat Gain Response: ± 0.3 dB Typical
- Single Supply Bias: 5 V @ 107 mA

AMMC-5618 Absolute Maximum Ratings [1]

Symbol	Parameters/ Conditions	Units	Min.	Max.
V_{D1}, V_{D2}	Drain Supply Voltage	V		7
V_{G1}	Optional Gate Voltage	V	-5	+1
V_{G2}	Optional Gate Voltage	V	-5	+1
I_{D1}	Drain Supply Current	mA		70
I_{D2}	Drain Supply Current	mA		84
P_{in}	RF Input Power	dBm		20
T_{ch}	Channel Temp.	°C		+150
T_b	Operating Backside Temp.	°C	-55	
T_{stg}	Storage Temp.	°C	-65	+165
T_{max}	Maximum Assembly Temp. (60 sec max)	°C		+300

Note:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

Note: These devices are ESD sensitive. The following precautions are strongly recommended:
Ensure that an ESD approved carrier is used when dice are transported from one destination to another.
Personal grounding is to be worn at all times when handling these devices.

AMMC-5618 DC Specifications / Physical Properties [1]

Symbol	Parameters and Test Conditions	Unit	Min.	Typical	Max.
V_{D1},V_{D2}	Recommended Drain Supply Voltage	V	3	5	7
I_{D1}	First stage Drain Supply Current (V_{D1}= 5V, V_{G1} = Open or Ground)	mA		48	
I_{D2}	Second stage Drain Supply Current (V_{D2}= 5V, V_{G2} = Open or Ground)	mA		59	
$I_{D1} + I_{D2}$	Total Drain Supply Current ($V_{G1} = V_{G2}$ = Open or Ground, $V_{D1}= V_{D2}$ = 5 V)	mA		107	140
θ_{ch-b}	Thermal Resistance [2] (Backside temperature (Tb) = 25°C	°C/W		22	

Notes:

1. Backside temperature T_b = 25°C unless otherwise noted
2. Channel-to-backside Thermal Resistance (θ_{ch-b}) = 32°C/W at $T_{channel}$ (T_c) = 150°C as measured using infrared microscopy. Thermal Resistance at backside temperature (T_b) = 25°C calculated from measured data.

AMMC-5618 RF Specifications [3, 5]

(T_b = 25°C, V_{DD}= 5 V, I_{DD} = 107 mA, Z_0 = 50 Ω)

Symbol	Parameters and Test Conditions	Unit	Min.	Typical	Max.
$\|S_{21}\|^2$	Small-signal Gain	dB	12.5	14.5	
$\Delta\|S_{21}\|^2$	Small-signal Gain Flatness	dB		± 0.3	
RL_{in}	Input Return Loss	dB	9	12	
RL_{out}	Output Return Loss	dB	9	12	
$\|S_{12}\|^2$	Isolation	dB	40	45	
P_{-1dB}	Output Power at 1dB Gain Compression @ 20 GHz	dBm	17.5	19.5	
P_{sat}	Saturated Output Power (3dB Gain Compression) @ 20 GHz	dBm		20.5	
OIP3	Output 3rd Order Intercept Point @ 20 GHz	dBm		26	
$\Delta S_{21} / \Delta T$	Temperature Coefficient of Gain [4]	dB/°C		-0.023	
NF	Noise Figure @ 20 GHz	dB		4.4	6.5

Notes:

3. 100% on-wafer RF test is done at frequency = 6, 13 and 20 GHz, except as noted.
4. Temperature Coefficient of Gain based on sample test
5. All tested parameters guaranteed with measurement accuracy ±1.5dB for S12, ±1dB for S11, S21, S22, P1dB and ±0.5dB for NF.

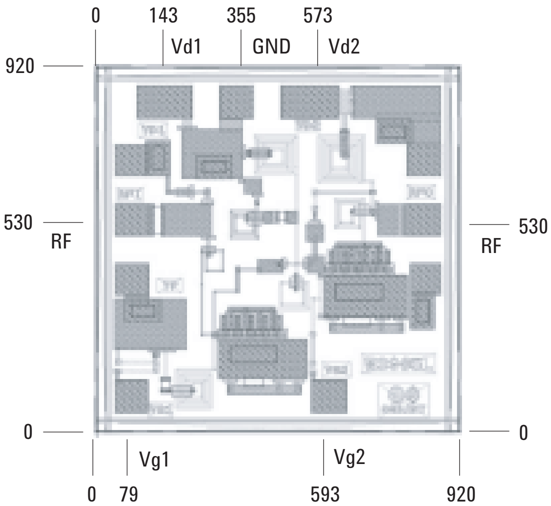

Figure 20. AMMC - 5618 Bond pad locations (dimensions in microns)

Ordering Information:

AMMC-5618-W10 = 10 devices per tray

AMMC-5618-W50 = 50 devices per tray